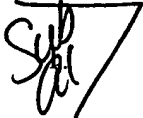


CLAIMS

What is claimed is:



1 A wide bandwidth phase-lock loop circuit, comprising:
2 a frequency detector arranged to detect frequency information of an input signal;
3 a frequency range selector connected to the frequency detector; and
4 a phase-locked loop connected to the frequency range selector and capable of
5 operating in a plurality of frequency ranges, wherein the frequency range selector
6 configures the phase-locked loop to generate an output signal within one of the plurality
7 of frequency ranges based on the frequency information of the input signal.

1 2. The circuit of claim 1, further comprising a divider connected to the
2 phase-locked loop and configurable to divide a frequency of the output signal generated
3 by the phase-locked loop.

1 3. The circuit of claim 1, wherein the frequency range selector employs
2 frequency range hysteresis.

1 4. The circuit of claim 1, wherein the frequency detector comprises a
2 zero-crossing synchronizer that synchronizes the input signal to a clock signal.

1 5. The circuit of claim 1, wherein the frequency detector comprises a
2 zero-crossing counter that counts zero-crossings of the input signal.

1 6. The circuit of claim 1, wherein the frequency range selector comprises
2 a range detector for detecting which one of the plurality of frequency ranges is an
3 appropriate frequency range based on the frequency information of the input signal.

1 7. The circuit of claim 6, wherein the frequency range selector further
2 comprises a range selector for confirming the frequency range detected by the range
3 detector.

1 8. The circuit of claim 1, further comprising a voltage comparator
2 connected to the frequency detector and adapted to condition a wave form of the input
3 signal.

1 9. A method of phase locking a signal having a wide range of frequencies,
2 comprising:
3 obtaining frequency information of an input signal;
4 selecting one out of a plurality of frequency ranges based on the frequency
5 information of the input signal; and
6 generating an output signal within the selected frequency range.

1 10. The method of claim 9, further comprising dividing a frequency of the
2 output signal.

1 11. The method of claim 9, further comprising employing frequency range
2 hysteresis.

1 12. The method of claim 9, further comprising confirming the selected
2 frequency range.

1 13. The method of claim 9, further comprising synchronizing the input
2 signal to a clock signal.

1 14. The method of claim 9, further comprising counting zero-crossings of
2 the input signal.

1 15. The method of claim 9, further comprising conditioning a wave form of
2 the input signal.

1 16. A phase-lock loop circuit having a wide bandwidth, comprising:
2 means for obtaining frequency information of an input signal;
3 means for selecting one out of a plurality of frequency ranges based on the
4 frequency information of the input signal; and
5 means for generating an output signal in the selected frequency range.

1 17. The circuit of claim 16, further comprising means for dividing a
2 frequency of the output signal.

1 18. The circuit of claim 16, wherein the means for selecting employs
2 frequency range hysteresis.

1 19. The circuit of claim 16, wherein the means for selecting confirms the
2 selected frequency range.

1 20. The circuit of claim 16, wherein the means for obtaining synchronizes
2 the input signal to a clock signal.

1 21. The circuit of claim 16, wherein the means for obtaining counts
2 zero-crossings of the input signal.

1 22. The circuit of claim 16, further comprising means for conditioning a
2 wave form the input signal.

- 1 23. A wide bandwidth phase-lock loop circuit, comprising:
- 2 a frequency detector arranged to detect frequency information of an input signal,
- 3 the frequency detector having a zero-crossing synchronizer for synchronizing the input
- 4 signal to a clock signal and a zero-crossing counter for counting zero-crossings of the
- 5 input signal;
- 6 a frequency range selector connected to the frequency detector and having a range
- 7 detector and a range selector, wherein the range detector detects which one of a plurality
- 8 of frequency ranges is an appropriate frequency range based on the frequency information
- 9 of the input signal, and wherein the range selector confirms the frequency range detected
- 10 by the range detector;
- 11 a phase-locked loop connected to the frequency range selector and configured by
- 12 the frequency range selector to generate an output signal in the frequency range detected
- 13 by the range detector, wherein the frequency range selector employs frequency range
- 14 hysteresis;
- 15 a divider for dividing a frequency of the output signal; and
- 16 a voltage comparator for conditioning a wave form of the input signal.